1.0 General Description

1.1 Scope

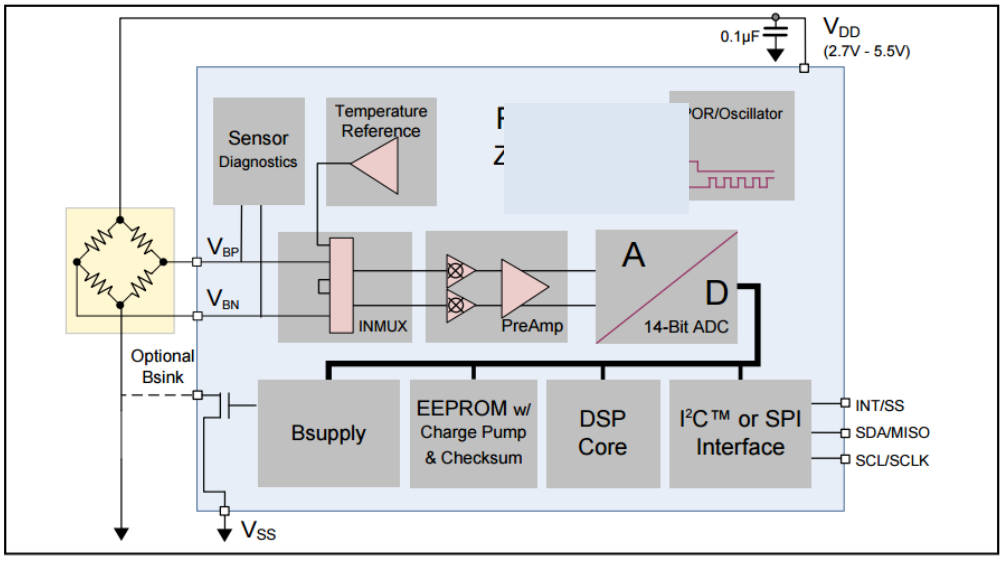
This application note is limited to AVSensors digital series pressure sensors with 14bit resolution. This includes the following product series. MCT-4D, MCT-5D, MCT-6D, MCT-SM58D, MCT-SM9333, MCT-SM9534.

1.2 Advanced Sensor, Multi Chip Technology, Digital Series

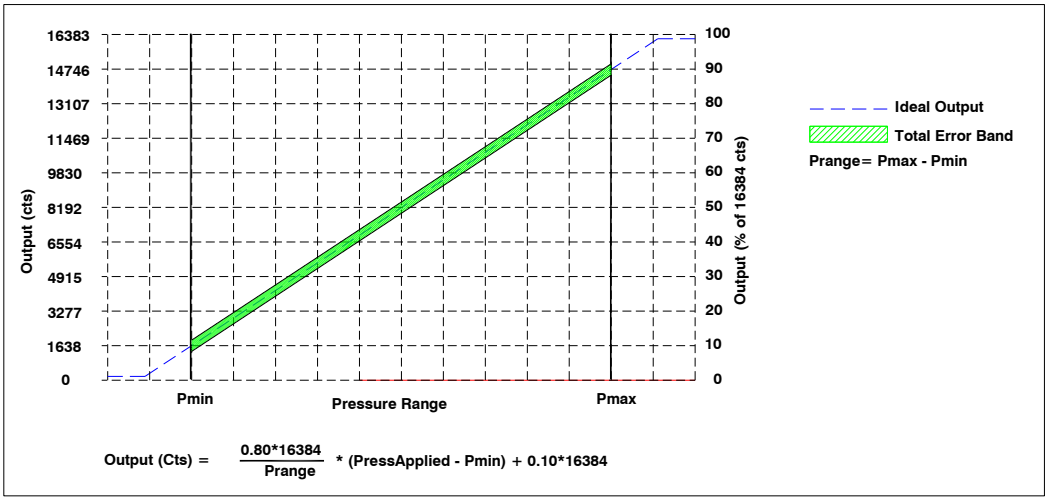
Advanced Sensors Multi Chip Technology (MCT) incorporates the latest mixed signal ASIC (Application Specific Integrated Circuit) with a bonded silicon gage to provide a leading *Digital Output* design for Industrial Transducers. The MCT Series provides a 14bit digital pressure and 11 bit digital temperature output offered in SPI and I^2C protocols. The rugged design is compatible with a wide range of harsh media including refrigerants, compressed air, and hydraulic fluids. The design superior performance provides 1% Total Error across a wide temperature range of -20 to 85°C and overall error of less than 2.5% over -40 to 125C. The flexible design incorporates many process fitting and connector types making it the ideal choice for OEM customers.

2.0 Block Diagram, Connections, Transfer Function

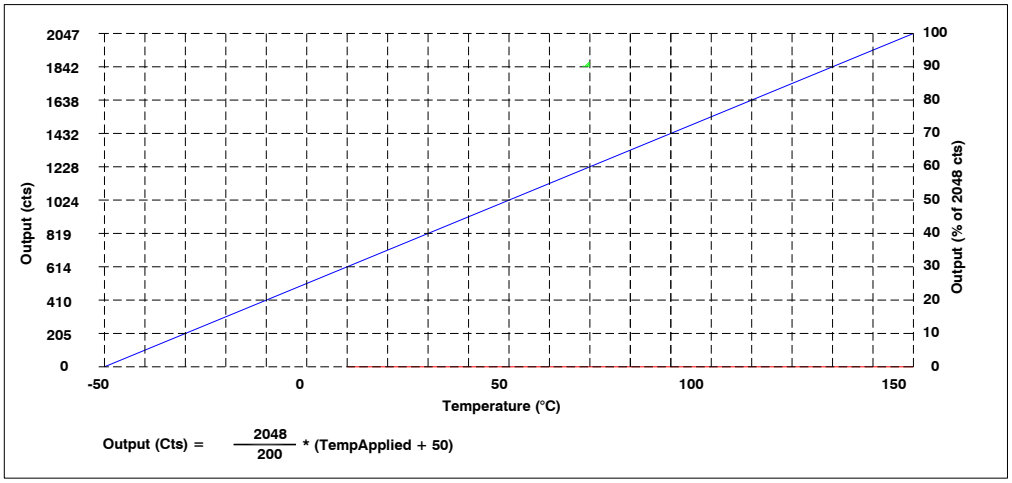
2.1 Block Diagram



2.2 Output Chart, Transfer Function, Pressure



2.2 Output Chart, Transfer Function, Temperature



3.0 Digital Protocols, I²C

3.1 I²C Summary

The I²C interface is a simple 8-bit protocol needing only two lines to communicate between a master and slave unit. The two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. . A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 1). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. In most cases, 4.7kΩ is a reasonable choice. The capacitive loads on SDA and SCL line have to be the same. It is important to avoid asymmetric capacitive loads. Data on the I²C -bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode. The number of interfaces connected to the bus is limited by the bus capacitance.

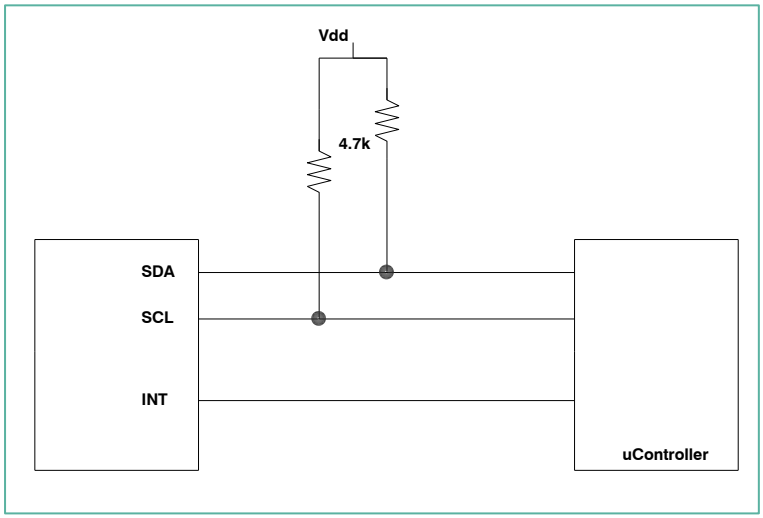


Figure 1, I²C *Interconnect with Pull Up Resistors*

3.2 Start & Stop Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P),. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. (Figure 2)

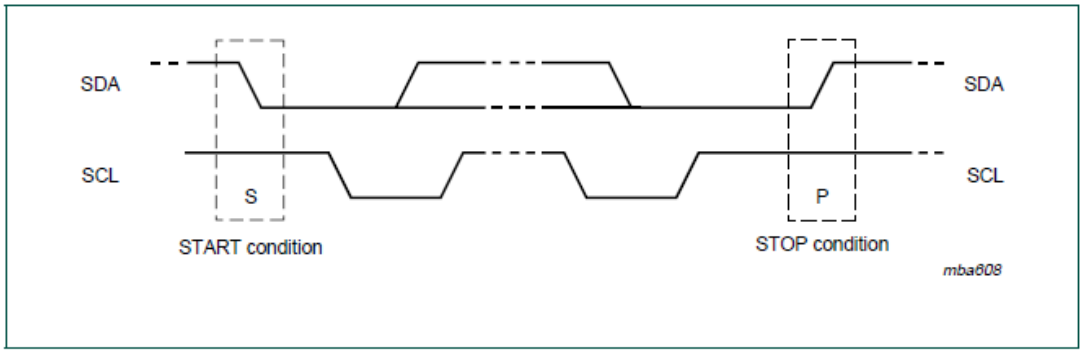


Figure 2, Start & Stop Conditions

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition..

3.3 Byte Format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first, (Figure 3). If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

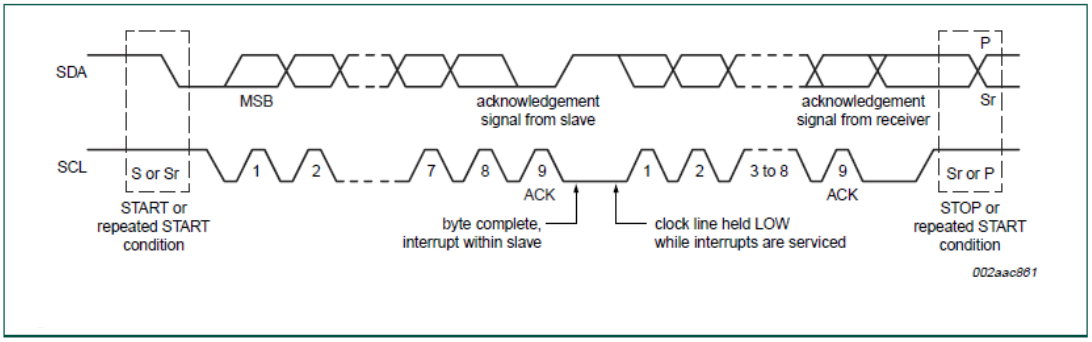


Figure 3, Data Transfer Format, Acknowledge

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses including the acknowledge, the 9th clock pulse, are generated by the master.

The Acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse. Set-up and hold times must also be taken into account.

When SDA remains HIGH during this 9th clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

3.4 Slave Address, Read & Write Bit

Data transfers follow the format shown below (Figure 4). After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W)—a ‘zero’ indicates a transmission (WRITE), a ‘one’ indicates a request for data (READ). (Figure 5)

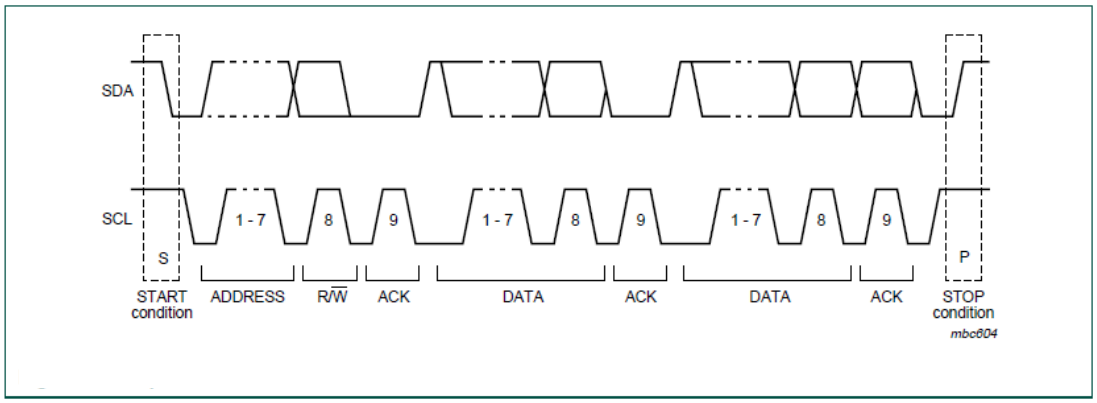


Figure 4, Complete Data Transfer Format

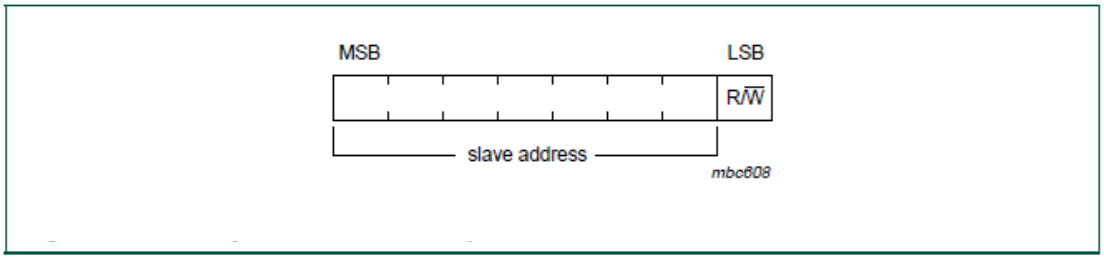


Figure 5, The first START byte

A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

3.5 INT/SS Pin

When programmed as an I^2C device, the INT/SS pin operates as an interrupt. The INT/SS pin rises when new output data is ready and falls when the next I^2C communication occurs. The INT/SS Pin can wire directly to the µController without pull up resistor.

3.6 I^2C Timing

The timing diagram and table show minimum and maximum transition times for specific conditions. (See Figure 6)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL clock frequency	f_{SCL}	100		400	kHz
Start condition hold time relative to SCL edge	t_{HDSTA}	0.1			µs
Minimum SCL clock low width [1)]	t_{LOW}	0.6			µs
Minimum SCL clock high width [1)]	t_{HIGH}	0.6			µs
Start condition setup time relative to SCL edge	t_{SUSTA}	0.1			µs
Data hold time on SDA relative to SCL edge	t_{HDDAT}	0			µs
Data setup time on SDA relative to SCL edge	t_{SUDAT}	0.1			µs
Stop condition setup time on SCL	t_{SUSTO}	0.1			µs
Bus free time between stop condition and start condition	t_{BUS}	2			µs

1) Combined low and high widths must equal or exceed minimum SCLK period.

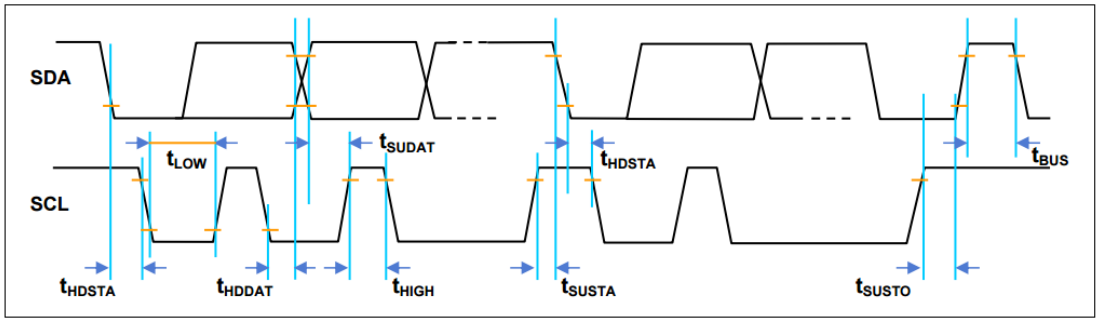


Figure 6, Timing and Transition Time Table

3.6 The Sensor Data Fetch Command Set

The sensor has four I²C read commands: Read_MR, Read_DF2, Read_DF3, and Read_DF4. Figure 7, below show the structure of the measurement packet of the four I²C read commands.

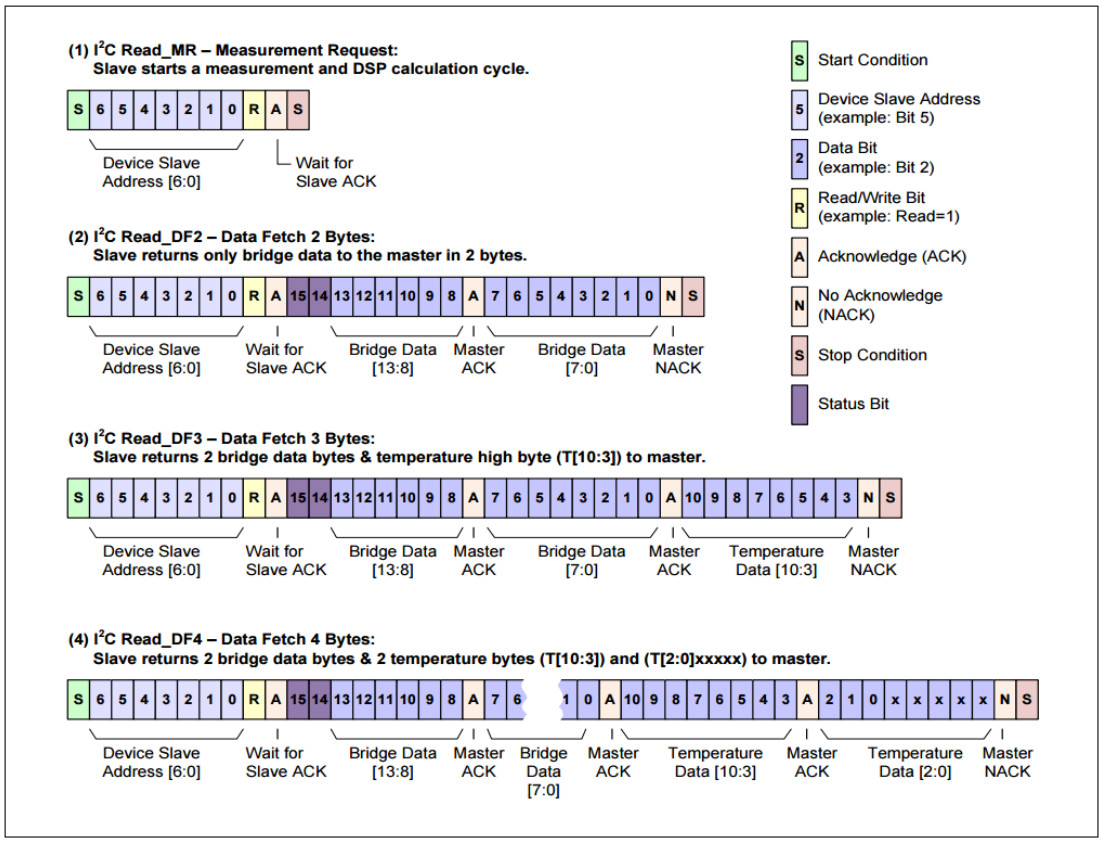


Figure 7, Complete Data Transfer Format

For Data Fetch commands, the number of data bytes returned by the sensor, is determined when the master sends the NACK and stop condition. For the Read_DF3 data fetch command, the sensor returns three bytes in response to the master sending the slave address and the READ bit (1): two bytes of bridge data with the two status bits as the MSBs and then 1 byte of temperature data (8-bit accuracy). After receiving the required number of data bytes, the master sends the NACK and stop condition to terminate the read operation. For the Read_DF4 command, the master delays sending the NACK and continues reading an additional final byte to acquire the full corrected 11-bit temperature measurement. In this case, the last 5 bits of the final byte of the packet are undetermined and should be masked off in the application. The Read_DF2 command is used if corrected temperature is not required. The master terminates the READ operation after the two bytes of bridge data.

The two status bits (Bit 15 and Bit 14) give an indication of stale or valid data depending on their value. A returned value of 00 indicate normal operation and a “Fresh” data packet” while a returned value of 10 indicates “Stale” data that has been already fetched”.. Users that use “status bit” polling should select a frequency slower than 20% more than the update time. For the highest code efficiency, using the interrupt polling (INT/SS) is best.

3.6 Status Bits

Figure 8 below, summarizes the status bits conditions indicated by the 2 MSB(Bit(15:14) of the I²C data packet or SPI data packet of the bridge high byte data.

Definition	Status Bits Bits 15 and 14
Normal Operation. Fresh Data Packet	00
Reserved	01
Stale Data. Data has been fetched since last measurement cycle.	10
Fault Detected	11

Figure 8, Status Bit Definition

All faults are detected in the next measurement cycle and reported in the subsequent data fetch. Once a fault is reported, the status bits will not change unless both the cause of the fault is fixed and a power- on-reset is performed.

3.7 Exceptions from the original I^2C Protocol

There are three differences in the described above protocol compared with original I^2C protocol:

1. Sending a start-stop condition without any transitions on the SCL line (no clock pulses in between) creates a communication error for the next communication, even if the next start condition is correct and the clock pulse is applied. An additional start condition must be sent, which results in restoration of proper communication.
2. The restart condition – a falling SDA edge during data transmission when the SCL clock line is still high – creates the same situation. The next communication fails, and an additional start condition must be sent for correct communication.
3. A falling SDA edge is not allowed between the start condition and the first rising SCL edge. If using an I^2C address with the first bit 0, SDA must be held down from the start condition through the first bit.

4.0 Digital Protocols, SPI

4.1 SPI Summary

SPI™ (Serial Peripheral Interface, introduced by Motorola) is a standard serial four wire synchronous data bus that can operate in full duplex. Devices communicate in master/slave mode with a single master initiating data frames. Multiple slave devices are allowed with individual slave select lines.

SPI specifies four signals: clock (SCLK); master data output, slave data input (MOSI); master data input, slave data output (MISO); and slave select (ÇSS). SCLK is generated by the master and input to all slaves. MOSI carries data from master to slave. MISO carries data from slave back to master. A slave device is selected when the master asserts its ÇSS signal.

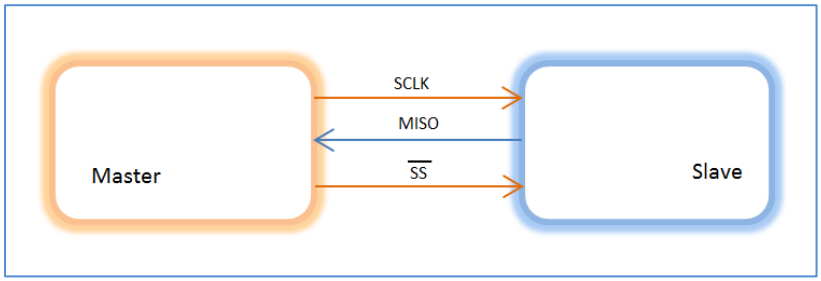


Figure 9, SPI Single Master, Half Duplex

Devices communicate using a master/slave relationship, in which the master initiates the data frame. When the master generates a clock and selects a slave device, data may be transferred in either or both directions simultaneously. In the implementation to the sensor, SPI is available only as half duplex or Read Only from the MCT Sensor. (See Figure 9)

4.1 SPI Read Operation

The MCT sensor's interface is programmed for falling edge MISO changes.

4.2 SPI Read Data Fetch

The SPI interface will have data change after the falling edge of SCLK. The master should sample MISO on the rise of SCLK. The entire output packet is 4 bytes (32 bits). The high bridge data byte comes first, followed by the low bridge data byte. Then 11 bits of corrected temperature (T[10:0]) are sent: first the T[10:3] byte and then the {T[2:0],xxxxx} byte. The last 5 bits of the final byte are undetermined and should be masked off in the application. If the user only requires the corrected bridge value, the read can be terminated after the 2nd byte. If the corrected temperature is also required but only at an 8-bit resolution, the read can be terminated after the 3rd byte is read. (See Figure 10)

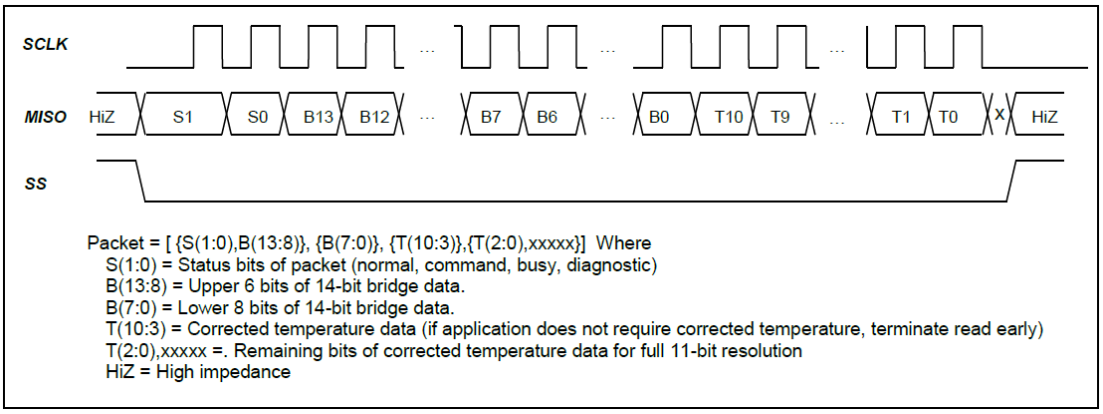


Figure 10, SPI Output Packet with Falling Edge SPI_Polarity

4.3 SPI Timing

The timing diagram and table below show minimum and maximum transition times for specific conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK clock frequency (4MHz clock)	f_{SCL}	50		800	kHz
SCLK clock frequency (1MHz clock)	f_{SCL}	50		200	kHz
SS drop to first clock edge	t_{HDSS}	2.5			µs
Minimum SCLK clock low width [1)]	t_{LOW}	0.6			µs
Minimum SCLK clock high width [1)]	t_{HIGH}	0.6			µs
Clock edge to data transition	t_{CLKD}	0		0.1	µs
Rise of SS relative to last clock edge	t_{SUSS}	0.1			µs
Bus free time between rise and fall of SS	t_{BUS}	2			µs

1) Combined low and high widths must equal or exceed minimum SCLK period.

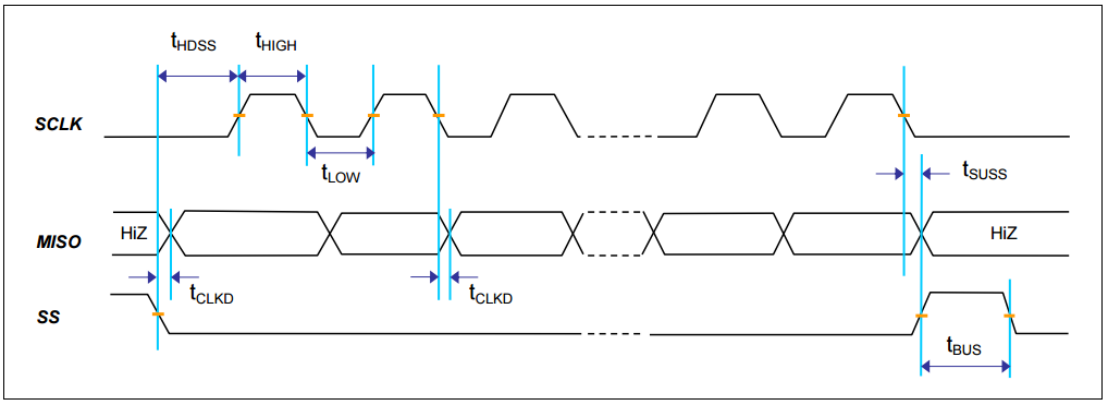


Figure 11, Timing and Transition Time Table